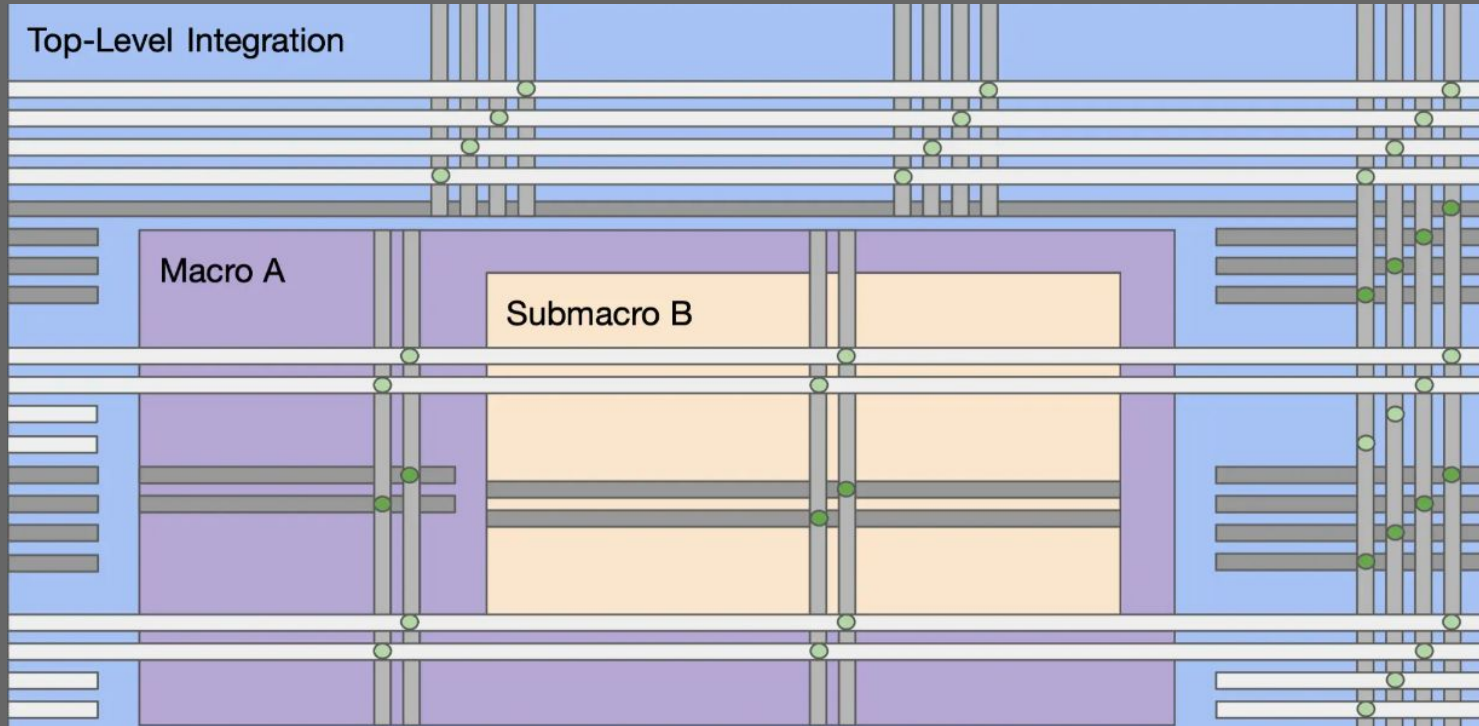


CPE 470 - Macros



Macro Dimensioning

- **Macros** are hand placed by designer
 - Unless using specialized tools
- Die Area is defined with set size
 - $[0, 0, x, y]$ creates x by y die size
 - $x \rightarrow$ width, $y \rightarrow$ height
- Macros placed in die using bottom left corner
 - Coordinates $[x1, y1]$ define bottom left corner placement
- Dimensions defined in **LEF** file

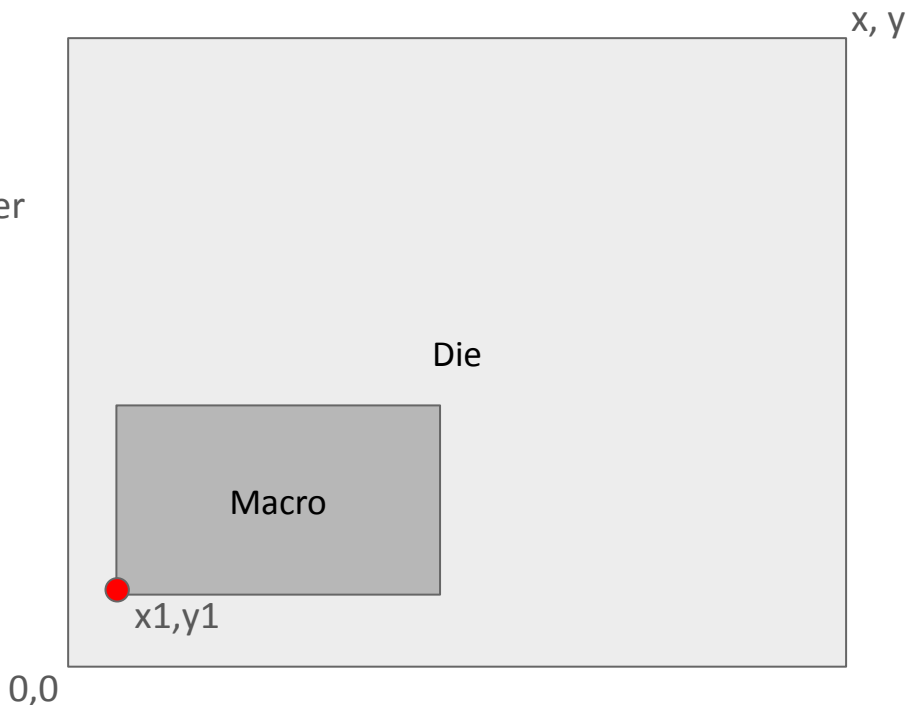
```
MACRO DFFRAM256x32
  CLASS BLOCK ;
  FOREIGN DFFRAM256x32 ;
  ORIGIN 0.000 0.000 ;
  SIZE 1152.795 BY 535.550 ;
```

x by y

Glossary

Macros: pre-laid-out blocks used by a design, similar to Hard IP

LEF: Library Exchange Format, defines dimensions and pin placement of macros



Rotation

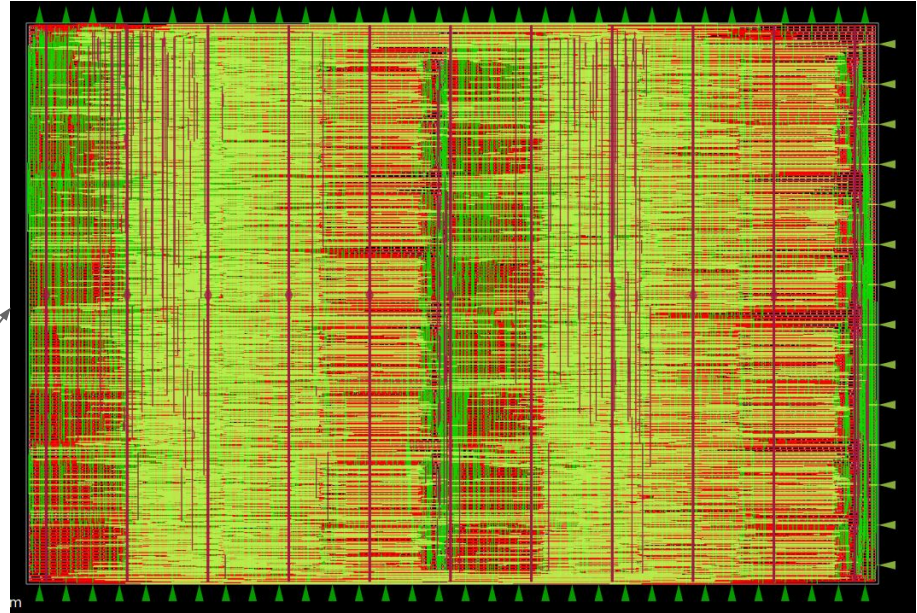
- Macros are rotated and flipped as needed
 - Used to get pins closer to where they are needed
 - Change shape to fit
- LEF Standard: Cardinal Directions define rotation
 - Most commonly North or South due to layer directionality
- Flipping generally mirrors over the Y axis

LEF/DEF	OpenAccess	Definition
N (North)	R0	
S (South)	R180	
W (West)	R90	
E (East)	R270	
FN (Flipped North)	MY	
FS (Flipped South)	MX	
FW (Flipped West)	MX90	
FE (Flipped East)	MY90	

Placement Considerations

- Where are the pins?
 - Pins should be rotated so that they are accessible
 - Not up against edge
- Macros near enough to edge
 - Center of chip most likely used for routing, logic
 - Not so close to edge as to be unroutable

Lack of pins on one side,
Could be placed right up
next to another macro



Multi Macro Considerations

Consider:

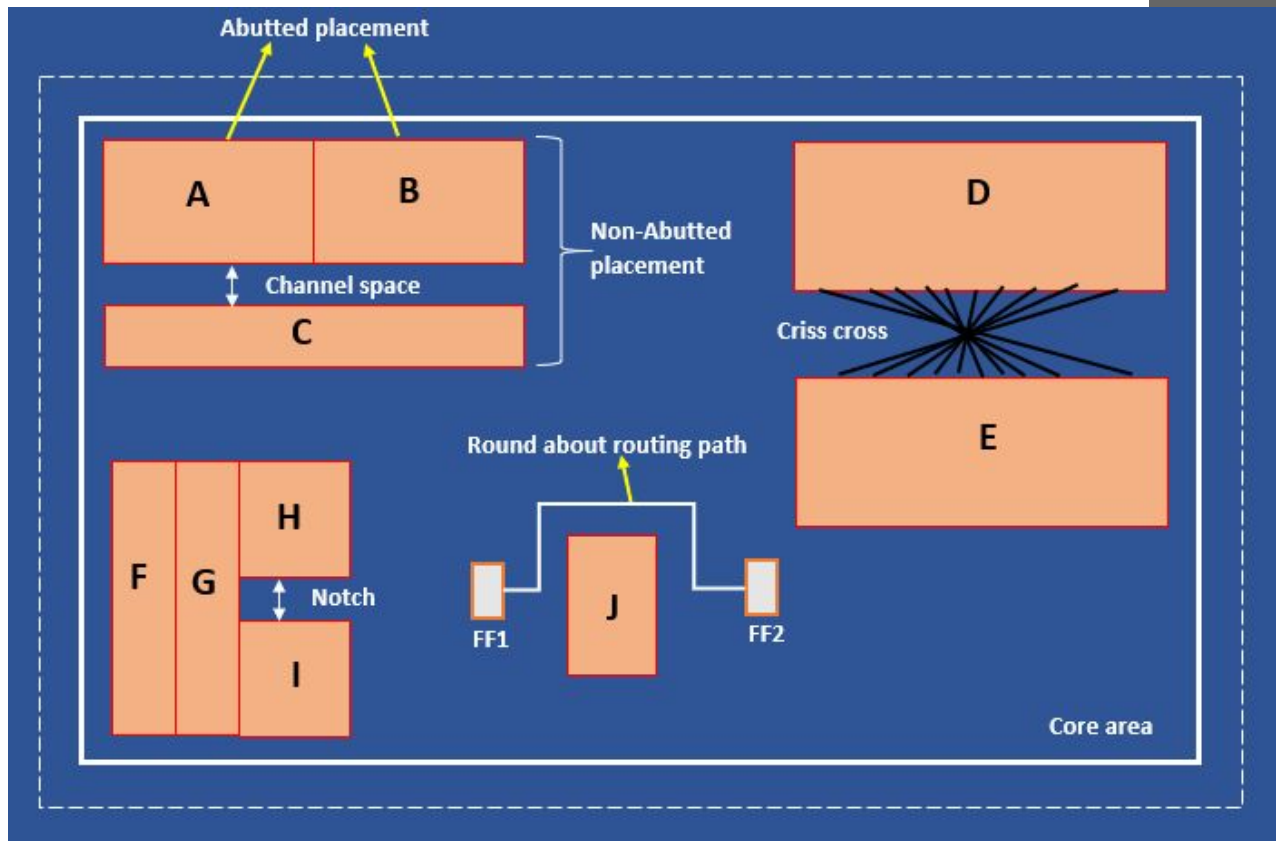
- + Channel Space
 - Often need room to route wires between macros
- + Abutted or Non-Abutted
 - No Pins on Side → Abutted saves area
 - Otherwise, need channels to route

Avoid:

- Notches
 - Creates Unusable Area
- Criss Cross
 - Difficult to Route
- Roundabout Paths
 - Don't place macros in highly congested areas

Glossary

Abutted: placed directly next to with no space in between



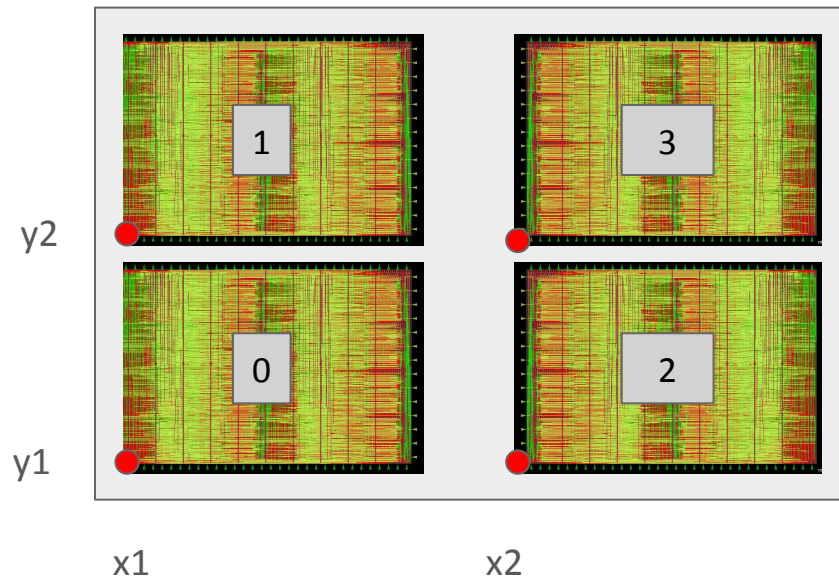
Placement Example

For example, Assume:

- DFFRAM macros are $1200 \times 600 \mu\text{m}$
- Minimum channel width of $100 \mu\text{m}$
- Center of die is to be kept free for routing
 - Start with a minimum central channel width (x) of $400 \mu\text{m}$
 - In this example, we have less room in the y direction

How do we lay out each macro?

What should our die area be?



Placement Example Solution

Rotations:

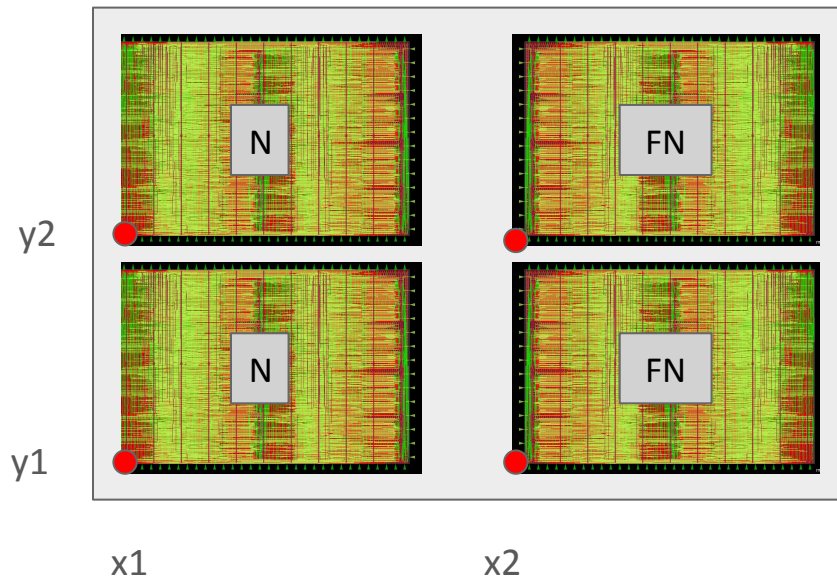
- Pin-free sides should face out
 - Left two macros → North (normal)
 - Right two macros → Flipped North

Die Area:

- Width: 2 macros + 2 Channels + 1 Central
 - $2*1200+2*100+400 = 3000$
- Height: 2 macros + 3 Channels
 - $2*600+3*100 = 1500$

Positions:

- X1 → 100 um (Channel width)
- X2 → 1700 um
 - Die - (macro + channel)
- Y1 → 100 um (Channel width)
- Y2 → 800 um
 - channel + macro + channel

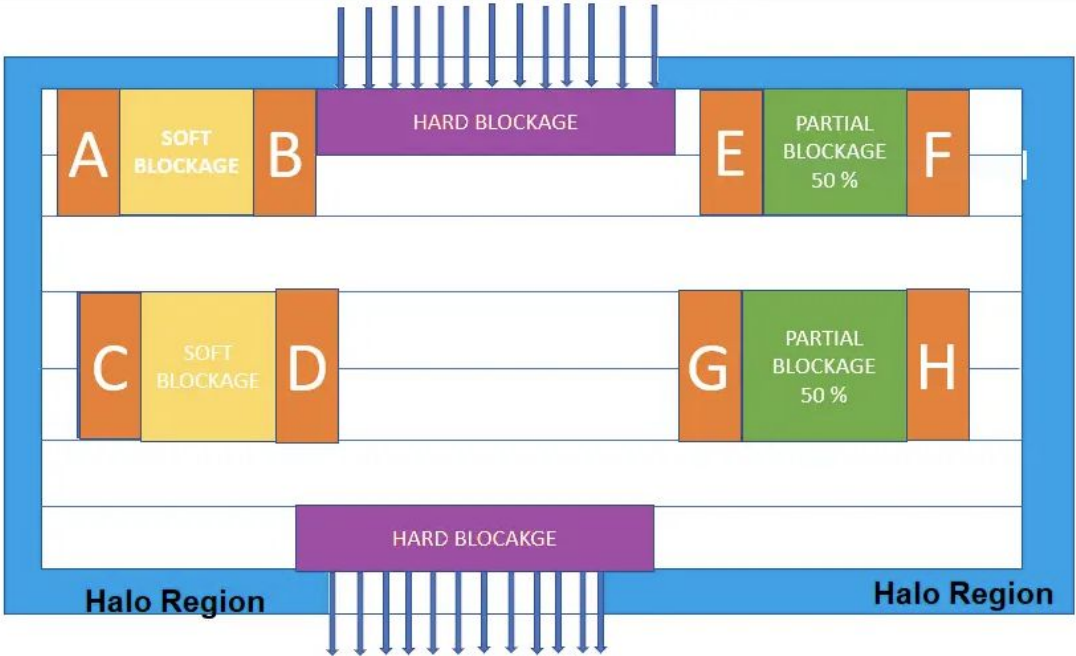


Halos and Blockages

- Macros are surrounded by **Halos** that prevent too-close cells
- Can configure **blockages** in high congestion areas
 - Prevent logic placement to make routing easier
- **Soft Blockage**: no standard cells can be placed, only buffers
 - Ideal in difficult to reach places where logic would be sub-optimal
- **Hard Blockage**: no cells can be placed
 - Ideal in areas of extremely high routing congestion, such as macro IO

Halo: area surrounding a macro that does not allow placement of standard cells

Blockage: places where cell placement is restricted



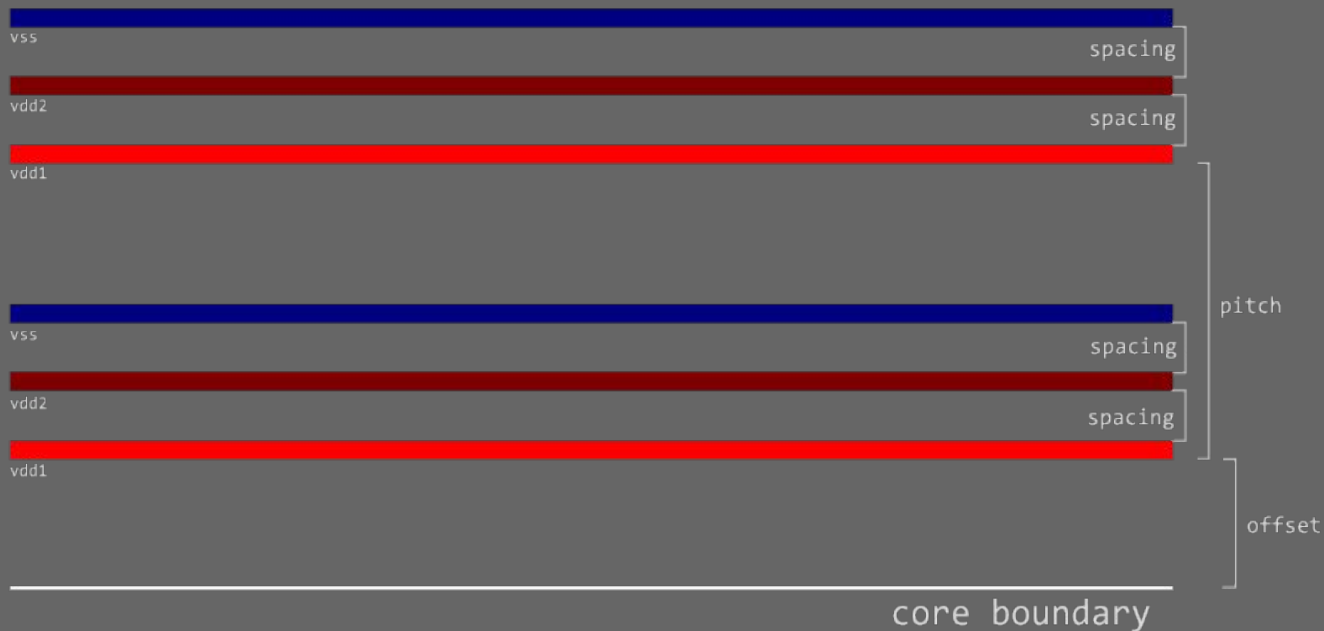
Power Straps

Glossary

Straps: wires that connect to power pads, existing on topmost metal layers

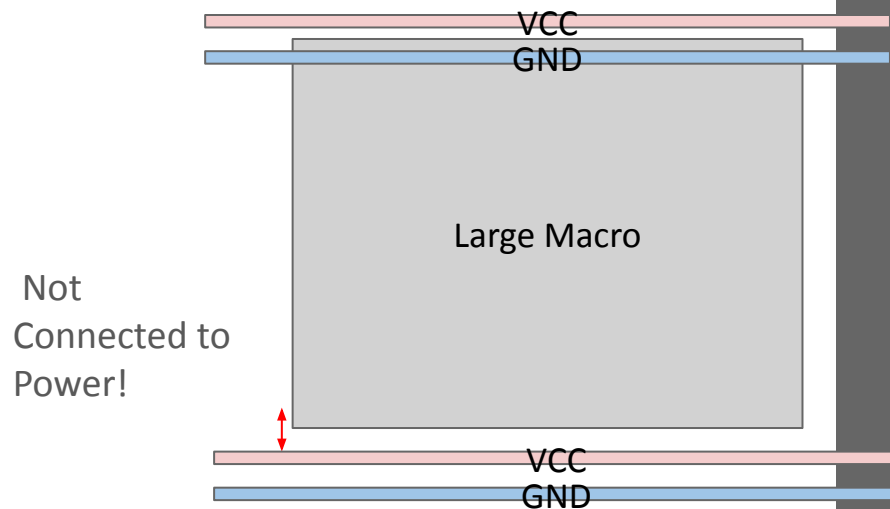
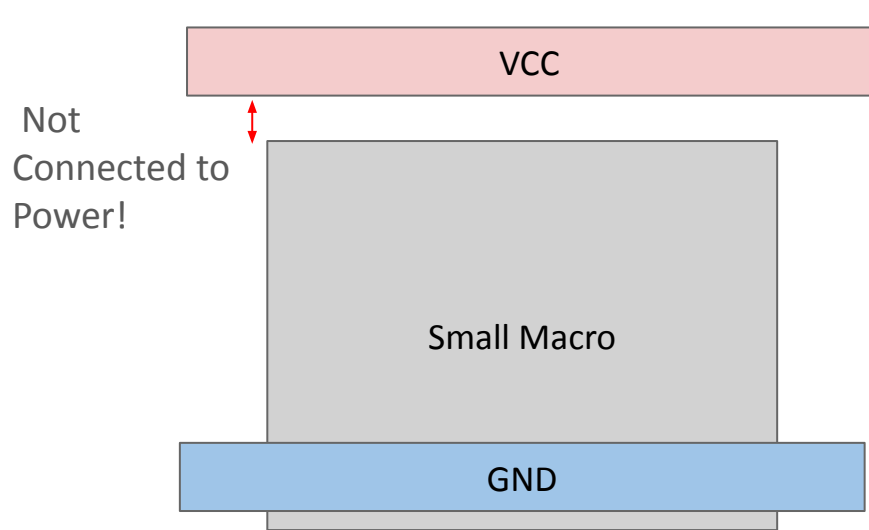
Spacing: distance between straps within a group

Pitch: distance between groups of straps



Power Distribution Network Integration

- Macros have their own PDN from when they were laid out
 - Have to connect our PDN to their PDN
- If either our PDN's spacing or pitch is too large, Macro won't get power
 - Solution → Lower spacing or pitch
 - Problem → leads to more power wires, less space for routing signals

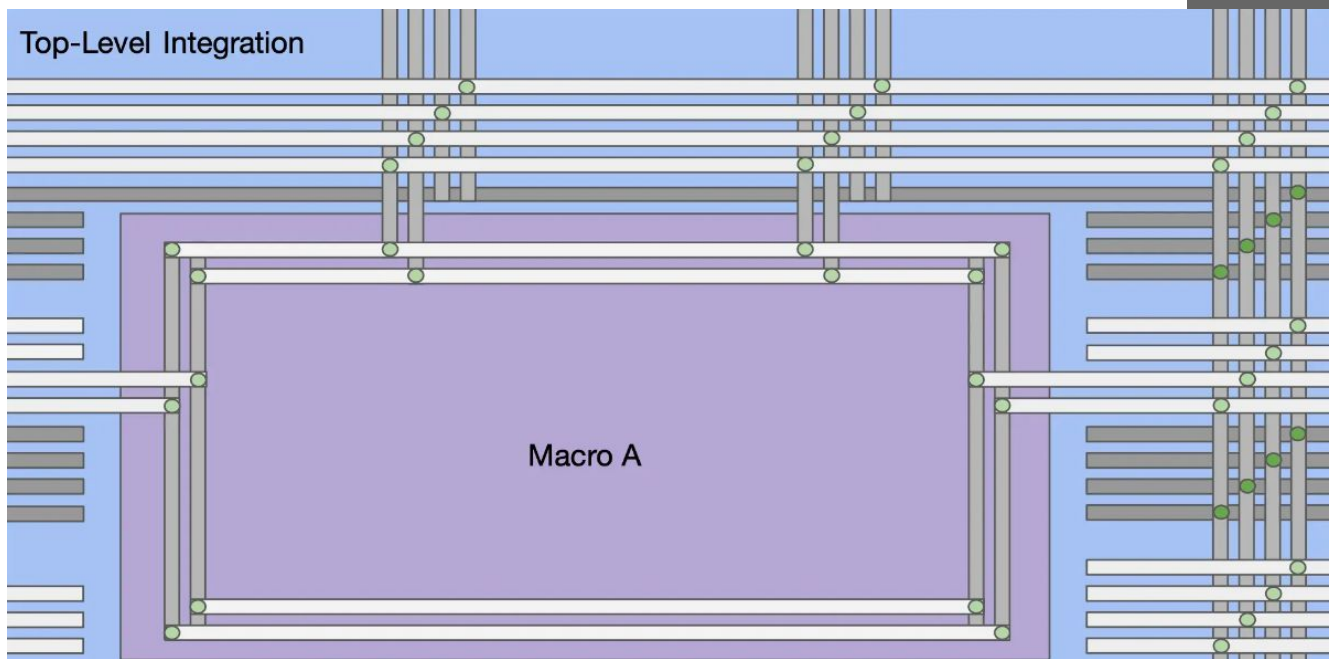


PDN Rings

- Macro PDN is shaped differently than top-level PDN
 - Need a way to integrate them
- Solution: Rings
 - Inside Ring, Macro has its own PDN
 - Ring provides attachment point
- Sacrifices Area
 - Ring is a border between two PDNs
 - Can't have logic under ring
 - Expands Halo

Glossary

Rings: top-level metal structures that surround a macro to connect its PDN to an outer PDN



PDN without Rings

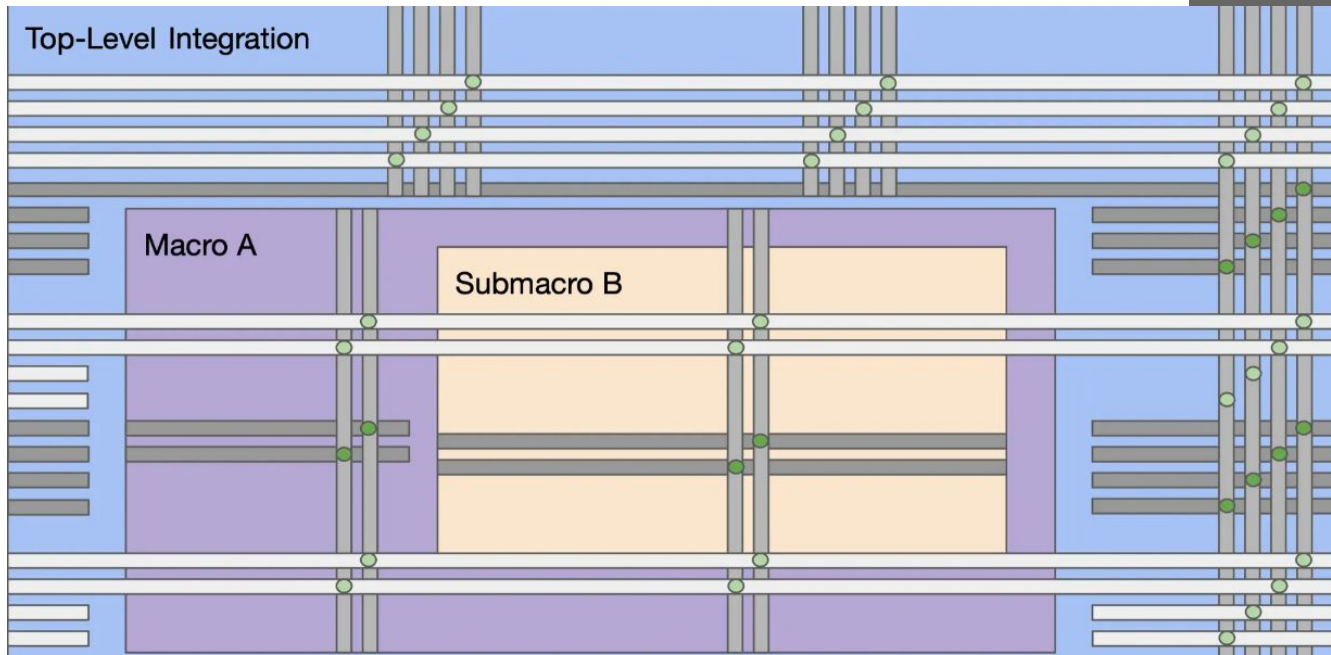
Glossary

Integrator: top-level PDN metal layer that connects to all macros

- Rings waste a lot of area around each macro, which adds up (especially with nested macros)
 - Instead, use a different top metal layer per macro
-
- Top level uses metal5 as integrator
 - Macro A cannot use metal 5 at all, uses metal4 for PDN
 - Macro B cannot use metal 4 or 5, uses metal3 for PDN

Tradeoffs:

- lose one routing layer per nested macro
- + don't lose as much area
- + Good for smaller macros



References

- <https://openlane2.readthedocs.io/en/latest/usage/pdn.html>
- <https://coriolis.lip6.fr/doc/lefdef/lefdefref/DEFSyntax.html>
- <https://vlsitalks.com/physical-design/floorplan/>
- <https://siliconvlsi.com/blockages-and-halos-in-vlsi/>
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